IN THE CLAIMS

1 (Currently Amended). A method comprising:

providing a register accessible by a plurality of ~~processors~~ central processing units; and

indicating whether data in said register is available for a given ~~processor~~ central processing unit.

2 (Currently Amended). The method of claim 1 including indicating for each of a plurality of ~~processors~~ central processing units whether the data is available for a given ~~processor~~ central processing unit.

3 (Currently Amended). The method of claim 2 including requiring a ~~processor~~ central processing unit to wait to execute an instruction until the data it needs to execute the instruction is available in one or more registers.

4 (Currently Amended). The method of claim 3 including providing a bit for each item of data indicating whether a given ~~processor~~ central processing unit can access that data.

5 (Currently Amended). The method of claim 4 including resetting said bit when said data is accessed by a given ~~processor~~ central processing unit.

6 (Currently Amended). The method of claim 5 including providing a register with a bit for each of a plurality ~~processors~~ of central processing units, enabling a ~~processor~~ central processing unit to reset said bit when the data is no longer useful to the ~~processor~~ central processing unit, and preventing any ~~processor~~ central processing unit from writing data to said register until all of the bits indicate that the data is no longer useful to any other ~~processor~~ central processing unit.

7 (Currently Amended). The method of claim 6 including indicating the ~~processor~~ central processing unit which will utilize the data written into the register.

8 (Currently Amended). The method of claim 1 includes enabling a plurality of ~~processors~~ central processing units to access a register at the same time.

9 (Currently Amended). The method of claim 1 including providing specialized ~~processors~~ central processing units for mathematical operations and for memory.

10 (Currently Amended). The method of claim 1 including providing an input ~~processor~~ central processing unit, an output ~~processor~~ central processing unit and coupling said input, output and specialized ~~processors~~ central processing units to said register through a cross-bar connection.

11 (Currently Amended). An article comprising a medium storing instructions that enable a processor-based system to:

make a register accessible by a plurality of central processing units ~~elements~~ in said system; and

indicate whether data in said register is available for a given processing ~~element~~ unit.

12 (Currently Amended). The article of claim 11 further storing instructions that enable the processor-based system to determine whether data is available in a register for a particular processing ~~element~~ unit.

13 (Original). The article of claim 12 further storing instructions that enable the processor-based system to prevent execution of an instruction until the data needed to execute the instruction is available in one or more registers.

14 (Currently Amended). The article of claim 13 further storing instructions that enable the processor-based system to check a bit in said register for each item of data indicating whether a processing ~~element~~ unit can access said data.

15 (Currently Amended). The article of claim 14 further storing instructions that enable the processor-based system to reset said bit when said data is accessed by a processing ~~element~~ unit.

16 (Currently Amended). The article of claim 15 further storing instructions that enable the processor-based system to identify in said register a bit for a processing ~~element~~ unit from among bits for a plurality of processing ~~elements~~ units, reset said bit when the data is no longer useful to a processing ~~element~~ unit, and to avoid writing said data to said register until all the bits indicate that the data is no longer useful to any other processing ~~element~~ unit.

17 (Currently Amended). The article of claim 16 further storing instructions that enable the processor-based system to indicate which processing ~~element~~ unit will utilize the data written into the register by another processing ~~element~~ unit.

18 (Currently Amended). A digital signal processor including:

a plurality of central processing ~~elements~~ units; and

a register coupled to said plurality of processing ~~elements~~ units, said register including a plurality of general purpose registers each accessible by said plurality of processing ~~elements~~ units, at least one of said registers indicating whether data in said register is available for a given one of said plurality of processing ~~elements~~ units.

19 (Currently Amended). The processor of claim 18 wherein said processing ~~elements~~ units are coupled to said register by a cross-bar connection.

20 (Currently Amended). The processor of claim 18 including a plurality of registers each including a bit indicating for each of said processing ~~elements~~ units whether the data in the general purpose register is available for a given processing ~~element~~ unit.

21 (Currently Amended). The processor of claim 18 wherein a processing ~~element~~ unit must wait to execute an instruction until the data it needs to execute the instruction is available in one or more general purpose registers.

22 (Currently Amended). The processor of claim 21 wherein each processing ~~element~~ unit has a designated bit for each general purpose register indicating whether a given processing ~~element~~ unit can access the data.

23 (Currently Amended). The processor of claim 18 wherein none of the processing ~~elements~~ units can write data to a general purpose register until all of the bits indicate that the data is no longer useful to any other processing ~~element~~ unit.

24 (Currently Amended). The processor of claim 18 including a plurality of general purpose registers, each of said general purpose registers including a data section and a storage area for a bit for each of said plurality of processing ~~elements~~ units.

25 (Currently Amended). The processor of claim 18 wherein said general purpose register is accessible by each of said processing ~~elements~~ units at the same time.

26 (Currently Amended). The processor of claim 18 wherein at least one of said processing ~~elements~~ units is an input processing ~~element~~ unit and another of said processing ~~element~~ unit an output processing ~~element~~ unit.

27 (Currently Amended). The processor of claim 26 further including at least one multiply and accumulate processing ~~element~~ unit.

28 (Original). The processor of claim 27 including at least one processing element for storing data in a random access memory.

29 (Original). The processor of claim 18 wherein no master processing element is included and instead, the sequence of operations in said digital signal processor is driven by the availability in a general purpose register of data needed to execute instructions.

30 (Currently Amended). The processor of claim 18 including a plurality of special purpose processing ~~elements~~ units that may each access a register at the same time.